



FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANTSATTY. DOCKET NO.
174/161 Cont.APPLICATION NO.
10/666,948APPLICANTS
Stephen J. Smith et al.CONFIRMATION NO.
7049FILING DATE
September 19, 2003GROUP ART UNIT
2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SKS	5,068,823	11/26/91	Robinson	395	500	
SKS	5,142,625	08/25/92	Nakai	395	275	
SKS	5,548,228	08/20/96	Madurawe	326	41	
SKS	5,535,342	07/09/96	Taylor	395	307	
SKS	5,684,980	11/04/97	Casselman	395	500	
SKS	5,966,534	10/12/99	Cooke et al.	395	705	
SKS	5,968,161	10/19/99	Southgate	712	37	
SKS	6,085,317	07/04/00	Smith	713	1	
SKS	6,282,627	08/28/01	Wong	712	15	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
SKS	1 444 084	07/28/76	Great Britain	H03K	19/00		
SKS	EP 0 419 105 A2	03/27/91	EPO	G06F	15/78		
SKS	EP 0 445 913 A2	09/11/91	EPO	G06F	15/60		
SKS	WO 94/10627	05/11/94	PCT	G06F	5/00		
SKS	EP 0 759 662 A2	02/26/97	EPO	H03K	19/177		
SKS	WO 97/13209	04/10/97	PCT	G06F	17/50		
SKS	EP 0 801 351 A2	10/15/97	EPO	G06F	13/12		
SKS	EP 0 829 812 A2	03/18/98	EPO	G06F	17/50		
SKS	WO 00/38087	06/29/00	PCT	G06F	17/50		

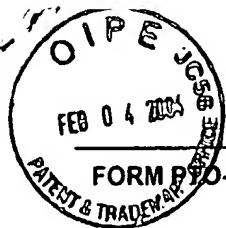
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
SKS	M. Wazlowski et al., "PRISM-II Compiler and Architecture," IEEE, 1993, pp. 9-16.
SKS	David Wo et al., "Compiling to the gate Level for a Reconfigurable Co-Processor," IEEE, 1994, pp. 147-154.
S	

EXAMINER Suresh K SuryawanshiDATE CONSIDERED 7/22/04

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Sheet 2 of 2

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EXAMINER INITIAL	
<i>SKS</i>	Christian Iseli et al., "A C++ compiler for FPGA custom execution units synthesis," IEEE, 1995, pp. 173-179.
<i>SKS</i>	Ian Page, "Constructing Hardware-Software Systems from a Single Description," Journal of VLSI Signal Processing, Vol. 12, No. 1, January 1996, pp. 87-107.
<i>SKS</i>	M.D. Edwards; J. Forrest - "Software acceleration using programmable hardware devices," January 1996, p. 55-63.
<i>SKS</i>	Tsuyoshi Isshiki et al., "Bit-Serial Pipeline Synthesis and Layout for Large-Scale Configurable Systems," IEEE, 1997, pp. 441-446.
<i>SKS</i>	Luc Séméria et al., "SpC: Synthesis of Pointers in C Application of Pointer Analysis to the Behavioral Synthesis from C," 1998, pp. 340-346.
<i>SKS</i>	ELECTRONIK, DE, FRANZIS VERLAG GMBH - "MIT PROGRAMMIERBARER LOGIK VERHEIRATED," March 31, 1998, Vol. 47, No. 7, p. 38.
<i>SKS</i>	Michael J. Wirthlin and Brad L. Hutchings - "Improving Functional Density Using Run-Time Circuit Reconfiguration," June 1998, p. 247-256.
<i>SKS</i>	João M.P. Cardoso et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," IEEE, 1999, pp. 2-11.
<i>SKS</i>	Bernardo Kastrup et al., "ConCISE: A Compiler-Driven CPLD-Based Instruction Set Accelerator," IEEE, 1999, pp. 92-101.
<i>SKS</i>	"List of FPGA-based Computing Machines," Steve Guccione, < http://www.io.com/~guccione/HW_list.html >, Last updated March 31, 1999.
<i>SKS</i>	Timothy J. Callahan et al., "The Garp Architecture and C Compiler," IEEE, April 2000, pp. 62-69.

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*Suresh K. Suryawanshi*DATE CONSIDERED *7/24/04*

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